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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,506	01/29/2001	Michihiro Ohsuge	053969/0125	7376

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EXAMINER	
KUMAR, PANKAJ	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,506	OHSUGE, MICHIHIRO	
	Examiner	Art Unit	
	Pankaj Kumar	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-11,15,16,18-20,25,27,28,30-32,36 and 37* is/are rejected.

7)☒ Claim(s) *4-6,12-14,17,21-24,26,29,33-35 and 38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Specification

2. The disclosure is objected to because of the following informalities:

Page 2 line 13 there seems to be a typographical error with "DS-WCDNA"

Maximum value retrieving portion recitations should be labeled as 13 (and not 7) in the specification as it is labeled as 13 in the drawings.

Appropriate correction is required.

Claim Objections

3. Claims 18-29 are objected to because of the following informalities: claim 18 is grammatically incorrect with: preparing means for preparing a profile removed a correlation power of the peak retrieved at preceding time by said maximum value retrieving means. It should probably be: preparing means for preparing a profile by removing a correlation power of the peak retrieved at a preceding time by said maximum value retrieving means

4. Claims 25, 29 are similarly grammatically incorrect.

5. Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 2, 3, 7, 8, 9, 10, 11, 15, 16, 18, 19, 20, 25, 27, 28, 30, 31, 32, 36, 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Sourour WO 99/35763.

8. As per claim 1, Sourour teaches a pattern generating circuit comprising: generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path (Sourour pages 8-10, fig. 7: assign delays block 779 assigns delays to correlations 771 logically based on the inputs 779 receives and the delayed correlation values are stored in 772; all of these function as the pattern generating means to track the multipath signals); and removing means for removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means (Sourour fig. 7: 774 removes the largest peak from the logical pattern of peaks in the delay profile in 773 which received data from 772).

9. As per claim 2, Sourour teaches a pattern generating circuit comprising: generating means for generating a logical pattern of correlated peak in a delay profile of a transmission path (Sourour pages 8-10, fig. 7: assign delays block 779 assigns delays to correlations 771 logically

based on the inputs 779 receives and the delayed correlation values are stored in 772; all of these function as the pattern generating means to track the multipath signals); and removing means for sequentially removing a power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak generated by said generating means (Sourour fig. 7: 774 removes the largest peak from the logical pattern of peaks in the delay profile in 773 which received data from 772; sequentially 774 removes, then 776 removes, then 777 removes).

10. As per claim 3, Sourour teaches a pattern generating circuit as set forth in claim 2, wherein said removing means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data (Sourour pg. 9-10 steps 1-6, step 4: largest c1(n)^2 select again), and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data (Sourour pg. 9-10: steps4-6, step 6: process repeated).

11. As per claim 7, Sourour teaches a pattern generating circuit as set forth in claim 2, wherein said logical pattern represent a peak shape in single path of the delay profile (Sourour figs. 1, 2, 5, 6, 7).

12. As per claim 8, Sourour teaches a pattern generating circuit as set forth in claim 2, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile (Sourour figs. 2, 6, 7: each l is a path).

13. As per claim 9, Sourour teaches a multi-path detection circuit for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising: generating means for generating a logic pattern of a correlated peak in said delay profile; and detection means for

detecting position of the correlated peak on the basis of the logical pattern of the correlated peak generated by said generating means. (discussed above)

14. As per claim 10, Sourour teaches a multi-path detection circuit as set forth in claim 9, wherein said detection means comprises removing means for sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and means for sequentially detecting the position of said correlated peak from the delay profile by removing the power component of the correlated peak by said removing means. (discussed above)

15. As per claim 11, Sourour teaches a multi-path detection circuit as set forth in claim 9, wherein said detection means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data. (discussed above)

16. As per claim 15, Sourour teaches a multi-path detection circuit as set forth in claim 9, wherein said logical pattern represent a peak shape in single path of the delay profile. (discussed above)

17. As per claim 16, Sourour teaches a multi-path detection circuit as set forth in claim 9, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile. (discussed above)

18. As per claim 18, Sourour teaches a multi-path detection circuit comprising: a matched filter outputting a correlated value of a spread code and a received signal (Sourour fig. 7: 771, 772, 773, 774, 776 in combination are operating as a matched filter); delay profile storing means

for storing a delay profile of a transmission path measured by said matched filter (Sourour fig. 7: 779); maximum value retrieving means for retrieving a maximum peak position and a peak level from said delay profile stored in said delay profile storing means (Sourour pages 9-10 steps 1-6); pattern generating means for sequentially generating logical patterns of correlated peaks on the basis of the leak level and peak position obtained from said maximum value retrieving means (Sourour fig. 7: output of the correlators); and preparing means for preparing a profile removed a correlation power of the peak retrieved at preceding time by said maximum value retrieving means (Sourour pgs. 9-10 steps 4-6); said maximum value retrieving means retrieves said maximum peak value and said peak level sequentially from the profile generated by said generating means (Sourour figs. 6, 7; pages 9-10 steps 1-6).

19. As per claim 19, Sourour teaches a multi-path detection circuit as set forth in claim 18, wherein said pattern generating means generates a logical pattern of the peak of preceding time on the basis of the peak level and the peak position obtained from the maximum value retrieving means, said generating means removes correlated power detecting precedingly from the delay profile using the logical pattern of the correlated data generated by said pattern generating means. (discussed above)

20. As per claim 20, Sourour teaches a multi-path detection circuit as set forth in claim 18, wherein said maximum value retrieving means obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data. (discussed above)

21. As per claim 25, Sourour teaches a multi-path detection circuit as set forth in claim 18, wherein said preparing means preparing a profile removed the correlated power of the peak retrieved preceding time by said maximum value retrieving means by rèmoving the logical pattern of the correlated peak generated by said pattern generating means from the delay profile data retrieved said maximum peak position and said peak level by said maximum value retrieving means. (discussed above)

22. As per claim 27, Sourour teaches a multi-path detection circuit as set forth in claim 18, wherein said logical pattern represents a peak shape in single path of said delay profile. (discussed above)

23. As per claim 28, Sourour teaches a multi-path detection circuit as set forth in claim 18, wherein said logical pattern represents a peak shape and a side lobe contained therein in single path of said delay profile. (discussed above)

24. As per claim 30, Sourour teaches a multi-path detection method for detecting a timing of multi-path by measuring a delay profile of a transmission path, comprising the steps of: generating a logical pattern of a correlated peak in a delay profile; and detecting a position of correlated peak on the basis of the generated logical pattern of said correlated peak. (discussed above)

25. As per claim 31, Sourour teaches a multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak position includes step of sequentially removing power component of the detected correlated peak from said delay profile using the logical pattern of said correlated peak and step of sequentially detecting the position of

said correlated peak from the delay profile removed the power component of the correlated peak. (discussed above)

26. As per claim 32, Sourour teaches a multi-path detection method as set forth in claim 30, wherein said step of detecting position of said correlated peak obtains a peak level and a peak position of second path from a profile removed correlated power of a first path from a delay profile data, and subsequently obtains a peak level and a peak position of third path from a profile removed correlated power of the second path from a delay profile data. (discussed above)

27. As per claim 36, Sourour teaches a multi-path detection method as set forth in claim 30, wherein said logical pattern represent a peak shape in single path of the delay profile. (discussed above)

28. As per claim 37, Sourour teaches a multi-path detection method as set forth in claim 30, wherein said logical pattern represents the peak shape and side lobe contained therein in single path of the delay profile. (discussed above)

Allowable Subject Matter

Claims 4, 5, 6, 12, 13, 14, 17, 21-24, 26, 29, 33, 34, 35, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pankaj Kumar whose telephone number is (571) 272-3011. The examiner can normally be reached on Mon, Tues, Wed and Thurs after 8AM to after 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PK

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PRIMARY EXAMINER